

1c841 U.S. PTO
09/638245
08/14/00

APPLICATION

FOR

UNITED STATES LETTERS PATENT

SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

Be it known that Christopher M. Hanna of Marlborough, Massachusetts has invented certain improvements in BTSC ENCODER of which the following description is a specification.

BTSC ENCODER

Field of the Invention

The present invention relates generally to stereophonic audio encoders used for television broadcasting. More particularly, the invention relates to a digital encoder for generating the audio signals used in the broadcast of stereophonic television signals in the United States and in other countries.

Background of the Invention

In the 1980's, the United States Federal Communications Commission (FCC) adopted new regulations covering the audio portion of television signals which permitted television programs to be broadcast and received with bichannel audio, e.g., stereophonic sound. In those regulations, the FCC recognized and gave special protection to a method of broadcasting additional audio channels endorsed by the Electronic Industries Association and the National Association of Broadcasters and called the Broadcast Television Systems Committee (BTSC) system. This well-known standard is sometimes referred to as Multichannel Television Sound (MTS) and is described in the FCC document entitled, MULTICHANNEL TELEVISION SOUND TRANSMISSION AND AUDIO PROCESSING REQUIREMENTS FOR THE BTSC SYSTEM (OET Bulletin No. 60, Revision A, February 1986), as well as in the document published by the Electronic Industries Association entitled, MULTICHANNEL TELEVISION SOUND BTSC SYSTEM RECOMMENDED PRACTICES (EIA Television Systems Bulletin No. 5, July 1985). Television signals generated according to the BTSC standard are referred to hereinafter as "BTSC signals".

The original monophonic television signals carried only a single channel of audio. Due to the configuration of the monophonic television signal and the need to

maintain compatibility with existing television sets, the stereophonic information was necessarily located in a higher frequency region of the BTSC signal making the stereophonic channel much noisier than the monophonic audio channel. This resulted in an inherently higher noise floor for the stereo signal than for the monophonic signal. The BTSC standard overcame this problem by defining an encoding system that provided additional signal processing for the stereophonic audio signal. Prior to broadcast of a BTSC signal by a television station, the audio portion of a television program is encoded in the manner prescribed by the BTSC standard, and upon reception of a BTSC signal a receiver (e.g., a television set) then decodes the audio portion in a complementary manner. This complementary encoding and decoding insures that the signal-to-noise ratio of the entire stereo audio signal is maintained at acceptable levels.

Figure 1 is a block diagram of a prior art BTSC encoding system, or more simply, a BTSC encoder 100, as defined by the BTSC standard. Encoder 100 receives left and right channel audio input signals (indicated in Figure 1 as "L" and "R", respectively) and generates therefrom a conditioned sum signal and an encoded difference signal. It should be appreciated that while the system of the prior art and that of the present invention is described as useful for encoding the left and right audio signals of a stereophonic signal that is subsequently transmitted as a television signal, the BTSC system also provides means to encode a separate audio signal, e.g., audio information in a different language, which is separated and selected by the end receiver. Further, noise reduction components of the BTSC encoding system can be used for other purposes besides television broadcast, such as for improving audio recordings.

System 100 includes an input section 110, a sum channel processing section 120, and a difference channel processing section 130. Input section 110 receives the left and right channel audio input signals and generates therefrom a sum signal (indicated in Figure 1 as "L+R") and a difference signal (indicated in Figure 1 as "L-R"). It is well known that for stereophonic signals, the sum signal L+R may be used by itself to provide monophonic audio reproduction and it is this signal that is decoded by existing

1 monophonic audio television sets to reproduce sound. In stereophonic sets, the sum and
2 difference signals can be added to and subtracted from one another to recover the
3 original two stereophonic signals (L) and (R). Input section 110 includes two signal
4 adders 112, 114. Adder 112 sums the left and right channel audio input signals to
5 generate the sum signal, and adder 114 subtracts the right channel audio input signal
6 from the left channel audio input signal to generate the difference signal. As described
7 above, the sum signal $L+R$ is transmitted through a transmission media with the same
8 signal to noise ratio as achieved with the prior monophonic signals. However, the
9 difference signal $L-R$ is transmitted through a very noisy channel, particularly at the
10 higher frequency portion of the relevant spectrum so that the decoded difference signal
11 has a poorer signal-to-noise ratio because of the noisy medium and reduced dynamic
12 range of the medium. The dynamic range is defined as the range of signals between the
13 level of the noise floor and the maximum level where signal saturation occurs. In the
14 difference signal channel the dynamic range decreases at higher frequencies.
15 Accordingly, the difference signal is subjected to additional processing than that of the
16 sum signal so that the dynamic range can be substantially preserved.

17 More particularly, the sum channel processing section 120 receives the sum
18 signal and generates therefrom the conditioned sum signal. Section 120 includes a $75\mu s$
19 preemphasis filter 122 and a bandlimiter 124. The sum signal is applied to the input of
20 filter 122 which generates therefrom an output signal that is applied to the input of
21 bandlimiter 124. The output signal generated by the latter is then the conditioned sum
22 signal.

23 The difference channel processing section 130 receives the difference signal and
24 generates therefrom the encoded difference signal. Section 130 includes a fixed
25 preemphasis filter 132 (shown implemented as a cascade of two filters 132a and 132b),
26 a variable gain amplifier 134 preferably in the form of a voltage-controlled amplifier,
27 a variable preemphasis/deemphasis filter (referred to hereinafter as a "variable emphasis
28 filter") 136, an overmodulation protector and bandlimiter 138, a fixed gain amplifier

1 140, a bandpass filter 142, an RMS level detector 144, a fixed gain amplifier 146, a
2 bandpass filter 148, an RMS level detector 150, and a reciprocal generator 152.

3 The difference signal is applied to the input of fixed preemphasis filter 132 which
4 generates therefrom an output signal that is applied via line 132d to an input terminal
5 of amplifier 134. An output signal generated by reciprocal generator 152 is applied via
6 line 152a to a gain control terminal of amplifier 134. Amplifier 134 generates an output
7 signal by amplifying the signal on line 132d using a gain that is proportional to the value
8 of the signal on line 152a. The output signal generated by amplifier 134 is applied via
9 line 134a to an input terminal of variable emphasis filter 136, and an output signal
10 generated by RMS detector 144 is applied via line 144a to a control terminal of filter
11 136. Variable emphasis filter 136 generates an output signal by preemphasizing or
12 deemphasizing the high frequency portions of the signal on line 134a under the control
13 of the signal on line 144a. The output signal generated by filter 136 is applied to the
14 input of overmodulation protector and bandlimiter 138 which generates therefrom the
15 encoded difference signal.

16 The encoded difference signal is applied via feedback path 138a to the inputs of
17 fixed gain amplifiers 140, 146, which amplify the encoded difference signal by Gain A
18 and Gain B, respectively. The amplified signal generated by amplifier 140 is applied
19 to an input of bandpass filter 142 which generates therefrom an output signal that is
20 applied to the input of RMS level detector 144. The latter generates an output signal
21 as a function of the RMS value of the input signal level received from filter 142. The
22 amplified signal generated by amplifier 146 is applied to the input of bandpass filter 148
23 which generates therefrom an output signal that is applied to the input of RMS level
24 detector 150. The latter generates an output signal as a function of the RMS value of
25 the input signal level received from filter 148. The output signal of detector 150 is
26 applied via line 150a to reciprocal generator 152, which generates a signal on line 152a
27 that is representative of the reciprocal of the value of the signal on line 150a. As stated

1 above, the output signals generated by RMS level detector 144 and reciprocal generator
2 152 are applied to filter 136 and amplifier 134, respectively.

3 As shown in Figure 1, the difference channel processing section 130 is
4 considerably more complex than the sum channel processing section 120. The additional
5 processing provided by the difference channel processing section 130, in combination
6 with complementary processing provided by a decoder (not shown) receiving a BTSC
7 signal, maintains the signal-to-noise ratio of the difference channel at acceptable levels
8 even in the presence of the higher noise floor associated with the transmission and
9 reception of the difference channel. Difference channel processing section 130
10 essentially generates the encoded difference signal by dynamically compressing, or
11 reducing the dynamic range of the difference signal so that the encoded signal may be
12 transmitted through the limited dynamic range transmission path associated with a BTSC
13 signal, and so that a decoder receiving the encoded signal may recover all the dynamic
14 range in the original difference signal by expanding the compressed difference signal in
15 a complementary fashion. The difference channel processing section 130 is a particular
16 form of the adaptive signal weighing system described in U.S. Patent No. 4,539,526,
17 which is known to be advantageous for transmitting a signal having a relatively large
18 dynamic range through a transmission path having a relatively narrow, frequency
19 dependent, dynamic range.

20 Briefly, the difference channel processing section may be thought of as including
21 a wide band compression unit 180 and a spectral compression unit 190. The wide band
22 compression unit 180 includes variable gain amplifier 134 preferably in the form of a
23 voltage controlled amplifier, and the components of the feedback path for generating the
24 control signal to amplifier 134 and comprising amplifier 146, band pass filter 148, RMS
25 level detector 150, and reciprocal generator 152. Band pass filter 148 has a relatively
26 wide pass band, weighted towards lower audio frequencies, so in operation the output
27 signal generated by filter 148 and applied to RMS level detector 150 is substantially
28 representative of the encoded difference signal. RMS level detector 150 therefore

1 generates an output signal on line 150a representative of a weighted average of the
2 energy level of the encoded difference signal, and reciprocal generator 152 generates
3 a signal on line 152a representative of the reciprocal of this weighted average. The
4 signal on line 152a controls the gain of amplifier 134, and since this gain is inversely
5 proportional to a weighted average (i.e., weighted towards lower audio frequencies) of
6 the energy level of the encoded difference signal, wide band compression unit 180
7 "compresses", or reduces the dynamic range, of the signal on line 132a by amplifying
8 signals having relatively low amplitudes and attenuating signals having relatively large
9 amplitudes.

10 The spectral compression unit 190 includes variable emphasis filter 136 and the
11 components of the feedback path generating a control signal to the filter 136 and
12 comprising amplifier 140, band pass filter 142 and RMS level detector 144. Unlike
13 filter 148, band pass filter 142 has a relatively narrow pass band that is weighted
14 towards higher audio frequencies. As is well known, the transmission medium
15 associated with the difference portion of the BTSC transmission system has a frequency
16 dependent dynamic range and the pass band of filter 142 is chosen to correspond to the
17 spectral portion of that transmission path having the narrowest dynamic range (i.e., the
18 higher frequency portion). In operation the output signal generated by filter 142 and
19 applied to RMS level detector 144 contains primarily the high frequency portions of the
20 encoded difference signal. RMS level detector 144 therefore generates an output signal
21 on line 144a representative of the energy level in the high frequency portions of the
22 encoded difference signal. This signal then controls the preemphasis/deemphasis applied
23 by variable emphasis filter 136 so in effect the spectral compression unit 190
24 dynamically compresses high frequency portions of the signal on line 134a by an amount
25 determined by the energy level in the high frequency portions of the encoded difference
26 signal as determined by the filter 142. The use of the spectral compression unit 190
27 thus provides additional signal compression towards the higher frequency portions of the
28 difference signal, which combines with the wideband compression provided by the

1 variable gain amplifier 134 to effectively cause more overall compression to take place
2 at high frequencies relative to the compression at lower frequencies. This is done
3 because the difference signal tends to be noisier in the higher frequency part of the
4 spectrum. When the encoded difference signal is decoded with a wideband expander
5 and a spectral expander in a decoder (not shown), respectively in a complementary
6 manner to the wide band compression unit 180 and spectral compression unit 190 of the
7 encoder, the signal-to-noise ratio of the L-R signal applied to the difference channel
8 processing section 130 will be substantially preserved.

9 The BTSC standard rigorously defines the desired operation of the 75 μ s
10 preemphasis filter 122, the fixed preemphasis filter 132, the variable emphasis filter
11 136, and the bandpass filters 142, 148, in terms of idealized analog filters. Specifically,
12 the BTSC standard provides a transfer function for each of these components and the
13 transfer functions are described in terms of mathematical representations of idealized
14 analog filters. The BTSC standard also defines the gain settings, Gain A and Gain B,
15 of amplifiers 140 and 146, respectively, and also defines the operation of amplifier 134,
16 RMS level detectors 144, 150, and reciprocal generator 152. The BTSC standard also
17 provides suggested guidelines for the operation of overmodulation protector and
18 bandlimiter 138 and bandlimiter 124. Specifically, bandlimiter 124 and the bandlimiter
19 portion of overmodulation protector and bandlimiter 138 are described as low pass filters
20 with cutoff frequencies of 15 kHz, and the overmodulation protection portion of
21 overmodulation protector and bandlimiter 138 is described as a threshold device that
22 limits the amplitude of the encoded difference signal to 100% of full modulation where
23 full modulation is the maximum permissible deviation level for modulating the audio
24 subcarrier in a television signal.

25 Since encoder 100 is defined in terms of mathematical descriptions of idealized
26 filters it may be thought of as an idealized or theoretical encoder, and those skilled in
27 the art will appreciate that it is virtually impossible to construct a physical realization
28 of a BTSC encoder that exactly matches the performance of theoretical encoder 100.

1 Therefore, it is expected that the performance of all BTSC encoders will deviate
2 somewhat from the theoretical ideal, and the BTSC standard defines maximum limits
3 on the acceptable amounts of deviation. For example, the BTSC standard states that a
4 BTSC encoder must provide at least 30 db of separation from 100 Hz to 8,000 Hz
5 where separation is a measure of how much a signal applied to only one of the left or
6 right channel's inputs appears erroneously in the other of the left or right channel's
7 outputs.

8 The BTSC standard also defines a composite stereophonic baseband signal
9 (referred to hereinafter as the "composite signal") that is used to generate the audio
10 portion of a BTSC signal. The composite signal is generated using the conditioned sum
11 signal, the encoded difference signal, and a tone signal, commonly referred to as the
12 "pilot tone" or simply as the "pilot", which is a sine wave at a frequency f_H where f_H
13 is equal to 15,734 Hz. The presence of the pilot in a received television signal indicates
14 to the receiver that the television signal is a BTSC signal rather than a monophonic or
15 other non-BTSC signal. The composite signal is generated by multiplying the encoded
16 difference signal by a waveform that oscillates at twice the pilot frequency according to
17 the cosine function $\cos(4\pi f_H t)$, where t is time, to generate an amplitude modulated,
18 double-sideband, suppressed carrier signal and by then adding to this signal the
19 conditioned sum signal and the pilot tone.

20 Figure 2 is a graph of the spectrum of the composite signal. In Figure 2 the
21 spectral band of interest containing the content of the conditioned sum signal (or the
22 "sum channel signal") is indicated as "L+R", the two spectral sidebands containing the
23 content of the frequency shifted encoded difference signal (or the "difference channel
24 signal") are each indicated as "L-R", and the pilot tone is indicated by the arrow at
25 frequency f_H . As shown in Figure 2, in the composite signal the encoded difference
26 signal is used at 100% of full modulation, the conditioned sum signal is used at 50% of
27 full modulation, and the pilot tone is used at 10% of full modulation.

1 Stereophonic television has been widely successful, and existing encoders have
2 performed admirably, however, virtually every BTSC encoder now in use has been built
3 using analog circuitry technology. These analog BTSC encoders, and particularly the
4 analog difference channel processing sections, due to their increased complexity have
5 been relatively difficult and expensive to construct. Due to the variability of analog
6 components, complex component selection and extensive calibration have been required
7 to produce acceptable analog difference channel processing sections. Further, the
8 tendency of analog components to drift, over time, away from their calibrated operating
9 points has also made it difficult to produce an analog difference channel processing
10 section that consistently and repeatably performs within a given tolerance. A digital
11 difference channel processing section, if one could be built, would not suffer from these
12 problems of component selection, calibration, and performance drift, and could
13 potentially provide increased performance.

14 Further, the analog nature of existing BTSC encoders has made them
15 inconvenient to use with newly developed, increasingly popular, digital equipment. For
16 example, television programs can now be stored using digital storage media such as a
17 hard disk or digital tape, rather than the traditional analog storage media, and in the
18 future increasing use will be made of digital storage media. Generating a BTSC signal
19 from a digitally stored program now requires converting the digital audio signals to
20 analog signals and then applying the analog signals to an analog BTSC encoder. A
21 digital BTSC encoder, if one could be built, could accept the digital audio signals
22 directly and could therefore be more easily integrated with other digital equipment.

23 While a digital BTSC encoder would potentially offer several advantages, there
24 is no simple way to construct an encoder using digital technology that is functionally
25 equivalent to the idealized encoder 100 defined by the BTSC standard. One problem
26 is that the BTSC standard defines all the critical components of idealized encoder 100
27 in terms of analog filter transfer functions. As is well known, while it is generally
28 possible to design a digital filter so that either the magnitude or the phase response of

1 the digital filter matches that of an analog filter, it is extremely difficult to match both
2 the amplitude and phase responses without requiring large amounts of processing
3 capacity for processing data sampled at very high sampling rates or without significantly
4 increasing the complexity of the digital filter. Without increasing either the sampling
5 frequency or the filter order, the amplitude response of a digital filter can normally only
6 be made to more closely match that of an analog filter at the expense of increasing the
7 disparity between the phase responses of the two filters, and vice versa. However, since
8 small errors in either amplitude or phase decrease the amount of separation provided by
9 BTSC encoders, it would be essential for a digital BTSC encoder to closely match both
10 the amplitude and phase responses of an idealized encoder of the type shown at 100 in
11 Figure 1.

12 For a digital BTSC encoder to provide acceptable performance, it is critical to
13 preserve the characteristics of the analog filters of an idealized encoder 100. Various
14 techniques exist for designing a digital filter to match the performance of an analog
15 filter; however, in general, none of these techniques produce a digital filter (of the same
16 order as the analog filter) having amplitude and phase responses that exactly match the
17 corresponding responses of the analog filter. Ideal encoder 100 is defined in terms of
18 analog transfer functions specified in the frequency domain, or the s-plane, and to
19 design a digital BTSC encoder, these transfer functions must be transformed to the z-
20 plane. Such a transformation may be performed as a "many-to-one" mapping from the
21 s-plane to the z-plane which attempts to preserve time domain characteristics. However,
22 in such a transformation the frequency domain responses are subject to aliasing and may
23 be altered significantly. Alternatively, the transformation may be performed as a "one-
24 to-one" mapping from the s-plane to the z-plane that compresses the entire s-plane into
25 the unit circle of the z-plane. However, such a compression suffers from the familiar
26 "frequency warping" between the analog and digital frequencies. Prewarping can be
27 employed to compensate for this frequency warping effect, however, prewarping does
28 not completely eliminate the deviations from the desired frequency response. These

1 problems would have to be overcome to produce a digital BTSC encoder that performs
2 well and is not unduly complex or expensive.

3 There is therefore a need for overcoming these difficulties and developing a
4 digital BTSC encoder.

5
6 Objects of the Invention

7 It is an object of the present invention to substantially reduce or overcome the
8 above-identified problems of the prior art.

9 Another object of the present invention is to provide an adaptive digital weighing
10 system.

11 Still another object of the present invention is to provide an adaptive digital
12 weighing system for encoding an electrical information signal of a predetermined
13 bandwidth so that the information signal can be recorded on or transmitted through a
14 dynamically-limited, frequency dependent channel having a narrower dynamically-
15 limited portion in a first spectral region than in at least one other spectral region of the
16 predetermined bandwidth.

17 And another object of the present invention is to provide a digital BTSC encoder.

18 Yet another object of the present invention is to provide a digital BTSC encoder
19 that prevents ticking, a problem that can arise with substantially zero input signal levels.

20 And another object of the present invention is to provide a digital BTSC encoder
21 that uses a sampling frequency that is a multiple of a pilot tone signal frequency of
22 15,734 Hz so as to prevent interference between the signal information of the encoded
23 signal with the pilot tone signal.

24 Still another object of the invention is to provide a digital BTSC encoder for
25 generating a conditioned sum signal and an encoded difference signal that include
26 substantially no signal energy at the pilot tone frequency of 15,734 Hz.

27 Yet another object of the present invention is to provide a digital BTSC encoder
28 including a sum channel processing section for generating the conditioned sum signal,

1 and a difference processing section for generating the encoded difference signal, the sum
2 channel processing section including devices for introducing compensatory phase errors
3 into the conditioned sum signal to compensate for any phase errors introduced into the
4 encoded difference signal by the difference channel processing section.

5 And another object of the present invention is to provide a digital BTSC encoder
6 including a digital variable emphasis unit, the unit including a digital variable emphasis
7 filter characterized by a variable coefficient transfer function, and the unit further
8 including a device for selecting the coefficients of the variable coefficient transfer
9 function as a function of the signal energy of the encoded difference signal.

10 Yet another object of the present invention is to provide a digital BTSC encoder
11 including a composite modulator for generating a composite modulated signal from the
12 conditioned sum signal and the encoded difference signal.

13 Still another object of the present invention is to provide a digital BTSC encoder
14 that may be implemented on a single integrated circuit.

15
16 **Summary of the Invention**

17 These and other objects are provided by an improved BTSC encoder that includes
18 an input section, a sum channel processing section, and a difference channel processing
19 section all of which are implemented using digital technology. In one aspect, the input
20 section includes high pass filters for preventing the BTSC encoder from exhibiting
21 "ticking". In another aspect, the BTSC encoder uses a sampling frequency that is equal
22 to an integer multiple of the pilot frequency.

23 In yet another aspect, the sum channel processing section generates a conditioned
24 sum signal, and the difference channel processing section generates an encoded
25 difference signal, and the sum channel processing section includes components for
26 introducing a phase error into the conditioned sum signal to compensate for any phase
27 errors introduced into the encoded difference signal by the difference channel processing
28 section.

1 According to yet another aspect, the invention provides an adaptive digital
2 weighing system for encoding an electrical information signal of a predetermined
3 bandwidth so that the information signal can be recorded on or transmitted through a
4 dynamically-limited, frequency dependent channel having a narrower dynamically-
5 limited portion in a first spectral region than in at least one other spectral region of the
6 predetermined bandwidth.

7 Still other objects and advantages of the present invention will become readily
8 apparent to those skilled in the art from the following detailed description wherein
9 several embodiments are shown and described, simply by way of illustration of the best
10 mode of the invention. As will be realized, the invention is capable of other and
11 different embodiments, and its several details are capable of modifications in various
12 respects, all without departing from the invention. Accordingly, the drawings and
13 description are to be regarded as illustrative in nature, and not in a restrictive or limiting
14 sense, with the scope of the application being indicated in the claims.

15 Brief Description of the Drawings

16 For a fuller understanding of the nature and objects of the present invention,
17 reference should be had to the following detailed description taken in connection with
18 the accompanying drawings in which the same reference numerals are used to indicate
19 the same or similar parts wherein:
20

21 Figure 1 shows a block diagram of a prior art idealized BTSC encoder;

22 Figure 2 shows a graph of the spectrum of the composite signal generated in
23 accordance with the BTSC standards;

24 Figure 3 shows a block diagram of one embodiment of a digital BTSC encoder
25 constructed according to the invention;

26 Figures 4A-C show block diagrams of low pass filters used in the digital BTSC
27 encoder shown in Figure 3;

1 Figure 5 shows a detailed block diagram of the wideband compression unit used
2 in the digital BTSC encoder shown in Figure 3;

3 Figure 6 shows a block diagram of the spectral compression unit used in the
4 digital BTSC encoder shown in Figure 3;

5 Figure 7 shows a flow chart used for calculating the filter coefficients of the
6 variable emphasis filter used in the spectral compression unit shown in Figure 6;

7 Figures 8A-D show block diagrams that illustrate signal scaling that may be used
8 to preserve resolution and decrease the chance of saturation in fixed point
9 implementations of digital BTSC encoders constructed according to the invention;

10 Figure 9 shows a detailed block diagram of the composite modulator shown in
11 Figures 8B-C; and

12 Figure 10 shows a block diagram of one preferred embodiment of sum and
13 difference channel processing sections that may be used in digital BTSC encoders
14 constructed according to the invention.

15 16 Detailed Description of the Drawings

17 Figure 3 is a block diagram of one embodiment of a digital BTSC encoder 200
18 constructed according to the invention. Digital encoder 200 is constructed to provide
19 performance that is functionally equivalent to the performance of idealized encoder 100
20 (shown in Figure 1). As with idealized encoder 100, digital encoder 200 receives the
21 left and right channel audio input signals and generates therefrom the conditioned sum
22 signal and the encoded difference signal, however, in digital encoder 200 these input and
23 output signals are digitally sampled signals rather than continuous analog signals.

24 The choice of sampling frequency f_s for the left and right channel audio input
25 signals significantly affects the design of digital encoder 200. In the preferred
26 embodiments, the sampling frequency f_s is chosen to be an integer multiple of the pilot
27 frequency f_H , so that $f_s = Nf_H$ where N is an integer, and in the most preferred
28 embodiments, N is selected to be greater than or equal to three. It is important for

1 encoder 200 to insure that the conditioned sum and encoded difference signals do not
2 contain enough energy at the pilot frequency f_H to interfere with the pilot tone that is
3 included in the composite signal. As will be discussed in greater detail below, it is
4 therefore desirable for at least some of the filters in digital encoder 200 to provide an
5 * exceptionally large degree of attenuation at the pilot frequency f_H , and this choice of
6 sampling frequency f_s simplifies the design of such filters.

7 Digital encoder 200 includes an input section 210, a sum channel processing
8 section 220 and a difference channel processing section 230. Rather than simply
9 implementing the difference channel processing section 230 using digital technology, all
10 three sections 210, 220, 230 are implemented entirely using digital technology. Many
11 of the individual components in digital encoder 200 respectively correspond to individual
12 components in idealized encoder 100. In general, the components of digital encoder 200
13 have been selected so that their amplitude responses closely match the respective
14 amplitude responses of their corresponding components in encoder 100. This often
15 results in there being a relatively large difference between the phase responses of
16 corresponding components. According to one aspect of the present invention, means
17 are provided in digital encoder 200 for compensating for or nullifying these phase
18 differences, or phase errors. As those skilled in the art will appreciate, relatively small
19 phase errors in the difference channel processing section 230 may be compensated for
20 by introducing similar phase errors in the sum channel processing section 220, and
21 implementing the sum channel processing section using digital technology simplifies the
22 introduction of such desired compensating phase errors.

23 The input section 210 of encoder 200 includes two high pass filters 212, 214,
24 and two signal adders 216, 218. The left channel digital audio input signal L is applied
25 to the input of high pass filter 212, the latter generating therefrom an output signal that
26 is applied to positive input terminals of adders 216, 218. The right channel audio input
27 signal R is applied to the input of high pass filter 214 which generates therefrom an
28 output signal that is applied to a positive input terminal of adder 216 and to a negative

1 input terminal of adder 218. Adder 216 generates a sum signal (indicated in Figure 3
2 as "L+R") by summing the output signals generated by filters 212 and 214. Adder 218
3 generates a difference signal (indicated in Figure 3 as "L-R") by subtracting the output
4 signal generated by filter 214 from the output signal generated by filter 212. Input
5 section 210 is therefore similar to input section 110 (shown in Figure 1) however,
6 section 210 additionally includes the two high pass filters 212, 214 and generates digital
7 sum and difference signals.

8 High pass filters 212, 214 preferably have substantially identical responses and
9 preferably remove D.C. components from the left and right channel audio input signals.
10 As will be discussed in greater detail below, this D.C. removal prevents encoder 200
11 from exhibiting a behavior referred to as "ticking". Since the audio information content
12 of the left and right channel audio input signals of interest is considered to be within a
13 frequency band between 50 Hz and 15,000 Hz, removal of D.C. components does not
14 interfere with the transmission of the information content of the audio signals. Filters
15 212, 214, therefore, preferably have a cutoff frequency below 50 Hz, and more
16 preferably have a cutoff frequency below 10 Hz so that they will not remove any audio
17 information contained in the audio input signals. Filters 212, 214 also preferably have
18 a flat magnitude response in their passband. In one preferred embodiment, filters 212,
19 214 are implemented as first order infinite impulse response (IIR) filters, each having
20 a transfer function $H(z)$ given by the formula shown in the following Equation (1).

$$H(z) = \frac{1 - z^{-1}}{1 + a_1 z^{-1}} \quad (1)$$

22 Referring again to Figure 3, the sum channel processing section 220 receives the
23 sum signal and generates therefrom the conditioned sum signal. In particular, the sum
24 signal is applied to a 75 μ s preemphasis filter 222. The filter 222 in turn generates an
25 output signal that is applied to a static phase equalization filter 228. The filter 228
26 generates an output signal that is applied to a low pass filter 224 of section 220 which
27 in turn generates the conditioned sum signal.

1 The 75 μ s preemphasis filter 222 provides signal processing that is partially
2 analogous to the filter 122 (shown in Figure 1) of idealized encoder 100. The amplitude
3 response of filter 222 is preferably selected to closely match that of filter 122. As will
4 be discussed further below, means are preferably provided in difference channel
5 processing section 230 for compensation for any differences in the phase responses of
6 filters 222 and 122. In one preferred embodiment, filter 222 is implemented as a first
7 order IIR filter having a transfer function $H(z)$ that is described by the formula shown
8 in the following Equation (2).

$$9 \quad H(z) = \frac{b_0 + b_1 z^{-1}}{1 + a_1 z^{-1}} \quad (2)$$

10 Static phase equalization filter 228 performs processing that is not directly
11 analogous to any of the components in idealized encoder 100 (shown in Figure 1). As
12 will be discussed in greater detail below, static phase equalization filter 228 is used to
13 introduce phase errors that compensate for phase errors introduced by difference
14 processing section 230. Briefly, static phase equalization filter 228 is preferably an "all-
15 pass" filter having a relatively flat amplitude response and a selected phase response.
16 In one preferred embodiment, filter 228 is implemented as a first order IIR filter having
17 a transfer function $H(z)$ that is described by the formula shown in the following
18 Equation (3).

$$19 \quad H(z) = \frac{a_0 + z^{-1}}{1 + a_0 z^{-1}} \quad (3)$$

20 Low pass filter 224 provides processing that is partially analogous to bandlimiter
21 124 (shown in Figure 1) of encoder 100. Low pass filter 224 preferably provides a flat
22 amplitude response in a pass band of zero to 15 kHz and a relatively sharp cutoff above
23 15kHz. Filter 224 also preferably provides an exceptionally large degree of attenuation
24 at the frequency f_H of the pilot tone (i.e., 15,734 Hz). By providing this exceptionally
25 large degree of attenuation, filter 224 insures that the conditioned sum signal does not

1 include enough energy at the pilot frequency f_H to interfere with the pilot tone used in
2 the composite signal. As discussed above, selecting the sampling frequency f_s to be
3 equal to an integer multiple of the pilot frequency f_H simplifies the design of a filter that
4 provides an exceptionally large degree of attenuation at the pilot frequency and therefore
5 simplifies the design of filter 224. Filter 224 preferably has a null at the pilot frequency
6 f_H and preferably provides at least 70 dB of attenuation for all frequencies from the pilot
7 frequency f_H up to one-half the sample rate.

8 Figure 4A is a block diagram illustrating one preferred embodiment of low pass
9 filter 224. As shown in Figure 4A, filter 224 may be implemented by cascading five
10 filter sections 310, 312, 314, 316, 318. In one preferred embodiment, all five filter
11 sections 310, 312, 314, 316, 318 are each implemented as a second order IIR filter
12 having transfer functions $H(z)$ which are described by the formula shown in the
13 following Equation (4).

$$14 \quad H(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}} \quad (4)$$

15 So in the embodiment shown in Fig. 4A, filter 224 is tenth order IIR filter.

16 Referring again to Figure 3, the difference channel processing section 230
17 receives the difference signal and generates therefrom the encoded difference signal.
18 The difference signal is applied to a low pass filter 238a which generates therefrom an
19 output signal that is applied to a fixed preemphasis filter 232a. The latter generates an
20 output signal that is applied via line 239 to an input terminal of a wideband compression
21 unit 280, and the encoded difference signal is applied via feedback line 240 to a detector
22 terminal of wideband compression unit 280. The latter generates an output signal that
23 is applied via line 281 to an input terminal of a spectral compression unit 290, and the
24 encoded difference signal is also applied via feedback line 240 to a detector terminal of
25 unit 290. The latter generates an output signal that is applied to a fixed preemphasis
26 filter 232b which in turn generates an output signal that is applied to a clipper 254.

1 Clipper 254 generates an output signal that is applied to a low pass filter 238b which
2 in turn generates the encoded difference signal.

3 Low pass filters 238a, 238b, together form a low pass filter 238 that performs
4 processing that is partially analogous to the bandlimiter portion of overmodulation
5 protector and bandlimiter 138 (shown in Figure 1) of idealized encoder 100. Preferably,
6 filter 238 is implemented so that it is substantially identical to low pass filter 224, which
7 is used in the sum channel processing section 220. Any phase errors introduced into the
8 encoded difference signal by filter 238 are therefore compensated by balancing phase
9 errors that are introduced into the conditioned sum signal by filter 224. Filter 238 is
10 preferably split into two sections 238a, 238b as shown for reasons which will be
11 discussed in greater detail below, and filter 238a preferably has a null at the pilot
12 frequency f_H .

13 Figures 4B-C are block diagrams illustrating one preferred embodiment of the
14 respective filters 238a and 238b. As shown in Figure 4B, filter 238a may be
15 implemented by cascading three filter sections 310, 314, 318 that are identical to three
16 of the filter sections used in filter 224 (shown in Figure 4A), and as shown in Figure
17 4C, filter 238b may be implemented by cascading two filter sections 312, 316 that are
18 identical to the two remaining sections used in filter 224.

19 Fixed preemphasis filters 232a, 232b (shown in Figure 3) together form a fixed
20 preemphasis filter 232 that performs processing that is partially analogous to filter 132
21 (shown in Figure 1) of idealized encoder 100. The amplitude response of filter 232 is
22 preferably selected to closely match the amplitude response of filter 132. In one
23 embodiment, the phase responses of filters 232 and 132 are significantly different, and
24 as will be discussed in greater detail below, the resulting phase errors are compensated
25 for by filters 222 and 228 in the sum channel processing section 220. Filter 232 is
26 preferably split into two sections 232a, 232b as shown for reasons that will be discussed
27 below. In one preferred embodiment, filters 232a, 232b are each implemented as first

1 order IIR filters having transfer functions $H(z)$ that are described by the formula shown
2 in Equation (2). So in this embodiment filter 232 is a second order IIR filter.

3 In one preferred embodiment, the difference between the phase responses of
4 filters 232b and 132a closely matches the difference between the phase responses of
5 filters 222 and 122. Therefore, the phase error introduced into the encoded difference
6 signal by fixed preemphasis filter 232b is balanced by the phase error introduced into
7 the conditioned sum signal by 75 μ s preemphasis filter 222. Further, in this
8 embodiment, the phase response of static phase equalization filter 228 is selected to
9 closely match the difference between the phase responses of fixed preemphasis filter
10 232a and filter 132b, so that any phase error introduced into the encoded difference
11 signal by filter 232a is balanced by a compensatory phase error in the conditioned sum
12 signal that is introduced by static phase equalization filter 228.

13 Clipper 254 performs processing that is partially analogous to the overmodulation
14 protection portion of overmodulation protector and bandlimiter 138 (shown in Figure 1)
15 used in idealized encoder 100. Briefly, clipper 254 is implemented as a thresholding
16 device, however, the operation of clipper 254 will be discussed in greater detail below.

17 Wideband compression unit 280 and spectral compression unit 290 perform
18 processing functions that are partially analogous to that of units 180 and 190,
19 respectively, of idealized encoder 100 (shown in Figure 1). Briefly, wideband
20 compression unit 280 dynamically compresses the signal on line 239 as a function of the
21 overall energy level in the encoded difference signal and spectral compression unit 290
22 further compresses high frequency portions of the signal on line 281 as a function of
23 high frequency energy in the encoded difference signal.

24 Figure 5 shows a block diagram of a preferred embodiment of a digital wideband
25 compression unit 280. Unit 280 includes a digital signal multiplier 434, a digital signal
26 multiplier 446, a wideband digital bandpass filter 448, a digital RMS level detector 450,
27 and a digital reciprocal generator 458. These components perform processing functions
28 partially analogous to those performed by amplifier 134, amplifier 146, bandpass filter

1 148, RMS level detector 150, and reciprocal generator 152, respectively, of idealized
2 encoder 100 (shown in Figure 1). The encoded difference signal is applied via feedback
3 path 240 to an input of wideband digital bandpass filter 448 which generates therefrom
4 an output signal that is applied to RMS level detector 450. The latter generates an
5 output signal that is representative of the RMS value of the output signal generated by
6 filter 448 and applies this output signal via line 450a to reciprocal generator 458.
7 Reciprocal generator 458 then generates an output signal representative of the reciprocal
8 of the signal on line 450a and applies this output signal via line 458a to multiplier 446.
9 Digital signal multiplier 446 multiplies the signal on line 458a by the value of the gain
10 setting, Gain D, and thereby generates an output signal that is representative of D times
11 the reciprocal of the RMS value and that is applied via line 446a to an input terminal
12 of multiplier 434. The output signal generated by fixed preemphasis filter 232a is
13 applied via line 239 to another input terminal of multiplier 434. Multiplier 434
14 multiplies the signal on line 239 by the signal on line 446a and thereby generates the
15 output of wideband compression unit 280 which is applied via line 281 to the input of
16 spectral compression unit 290.

17 Wideband digital bandpass filter 448 is designed to have an amplitude response
18 that closely matches the amplitude response of bandpass filter 148 (shown in Figure 1).
19 One preferred choice is to select filter 448 so that the mean square difference between
20 its amplitude response and that of filter 148 are minimized. In one embodiment, the
21 phase response of filters 448 and 148 are substantially different, but since the output
22 signal of the RMS level detector 450 is substantially insensitive to the phase of its input
23 signal, these phase differences may be ignored. In one preferred embodiment, wideband
24 bandpass filter 448 is implemented as a second order IIR filter having a transfer function
25 $H(z)$ that is described by the formula shown in Equation (4).

26 RMS level detector 450 is designed to approximate the performance of detector
27 150 which is used in idealized encoder 100 (shown in Figure 1). Detector 450 includes
28 a signal squaring device 452, a signal averaging device 454, and a square root device

1 456. Squaring device 452 squares the signal generated by bandpass filter 448 and
2 applies this squared signal via line 452a to averaging device 454. The latter computes
3 a time weighted average of the signal on line 452a and applies the average via line 454a
4 to square root device 456. Square root device 456 calculates the square root of the
5 signal on line 454a and thereby generates a signal on line 450a representative of the
6 RMS value of the output signal generated by wideband digital bandpass filter 448.

7 Averaging device 454 includes a digital signal multiplier 460, a digital signal
8 adder 462, a digital signal multiplier 464, and a delay register 465. The output signal
9 generated by squaring device 452 is applied via line 452a to one input of multiplier 460
10 which generates an output signal by scaling the signal on line 452a by a constant α .
11 The scaled output signal generated by multiplier 460 is applied to one input of adder 462
12 and an output signal generated by delay register 465 is applied to the other input of
13 adder 462. Adder 462 generates an output signal by summing the signals present at its
14 two inputs, and this summed signal is the output signal of averaging device 454 and is
15 applied to square root device 456 via line 454a. This summed signal is also applied to
16 one input of multiplier 464 which generates an output signal by scaling the summed
17 signal by the constant $(1-\alpha)$. The output signal generated by multiplier 464 is applied
18 to an input of delay register 465. Those skilled in the art will appreciate that averager
19 454 is a recursive filter and implements a digital averaging function that is described by
20 the recursive formula shown in the following Equation (5).

$$y(n) = \alpha x(n) + (1 - \alpha)y(n-1) \quad (5)$$

24 in which $y(n)$ represents the current digital sample of the signal output by averager 454
25 on line 454a, $y(n-1)$ represents the previous digital sample of the signal output by
26 averager 454 on line 454a, and $x(n)$ represents the current digital sample of the signal
27 output by squaring device 452 on line 452a. Those skilled in the art will appreciate that
28 averager 454 provides a digital approximation of the analog averaging function defined

1 in the BTSC standard and implemented by RMS level detector 150 (shown in Figure 1)
2 of idealized encoder 100. The constant α is preferably chosen so that the time constant
3 of RMS level detector 450 closely approximates the corresponding time constant
4 specified in the BTSC standard for RMS level detector 150.

5 Digital square root device 456 and digital reciprocal generator 458 are shown in
6 Figure 5 as two separate components, however, those skilled in the art will appreciate
7 that these two components may be implemented using a single device that generates an
8 output signal representative of the reciprocal of the square root of its input signal. Such
9 a device may be implemented for example as a memory look up table (LUT), or
10 alternatively may be implemented using processing components that calculate a Taylor
11 series polynomial approximation of the inverse square root function.

12 Figure 6 shows a block diagram of a preferred embodiment of spectral
13 compression unit 290. Unit 290 includes a variable preemphasis/deemphasis unit
14 (hereinafter referred to as the "variable emphasis unit") 536, a signal multiplier 540, a
15 spectral band pass filter 542, and an RMS level detector 544, and these components
16 provide processing which is partially analogous to that of variable emphasis filter 136,
17 amplifier 140, bandpass filter 142, and RMS level detector 144, respectively, of
18 idealized encoder 100 (shown in Figure 1). The encoded difference signal is applied via
19 feedback line 240 to an input of signal multiplier 540 which generates an output signal
20 by multiplying the encoded difference signal by the fixed gain setting value of Gain C.
21 The amplified output signal generated by signal multiplier 540 is applied to spectral
22 bandpass filter 542 which generates an output signal that is applied to RMS level
23 detector 544. The latter generates an output signal that is applied via line 544a to a
24 control terminal of variable emphasis unit 536, and the output signal generated by
25 wideband compressor unit 280 is applied via line 281 to an input terminal of unit 536.
26 The latter dynamically varies the frequency response applied to the signal on line 281
27 according to a function of the signal on line 544a, the latter signal being a function of
28 the signal energy of the encoded difference signal within the frequency band passed by

1 spectral band pass filter 542. The output signal of unit 290, which is generated by unit
2 536 and is applied to the input of fixed preemphasis filter 232b, is thus dynamically
3 compressed a greater amount in the high frequency portions of the signal than in the
4 remainder of the spectrum of interest.

5 Spectral bandpass filter 542 is designed to have an amplitude response that
6 closely matches the amplitude response of bandpass filter 142 (shown in Figure 1) of
7 idealized encoder 100. As with filter 448 (shown in Figure 5), one preferred choice is
8 to select filter 542 so that the difference between its RMS amplitude response and that
9 of filter 142 are minimized. In one embodiment, the phase response of filters 542 and
10 142 are substantially different, but since the RMS output of RMS level detector 544 is
11 substantially insensitive to the phase of the input to the detector, these phase differences
12 may be ignored. In one preferred embodiment, spectral bandpass filter 542 is
13 implemented as a cascade of three second order IIR filter sections 542a, 542b, 542c (as
14 shown in Figure 6) each having a transfer function $H(z)$ that is described by the formula
15 shown in Equation (4).

16 RMS level detector 544 is designed to approximate the performance of detector
17 144 which is used in idealized encoder 100 (shown in Figure 1). Detector 544 includes
18 a signal squaring device 552, a signal averaging device 554, and a square root device
19 556. Squaring device 552 squares the signal generated by spectral bandpass filter 542
20 and applies this squared signal via line 552a to averaging device 554. The latter
21 functions similarly to averaging device 454 (shown in Figure 5) which is used in the
22 wideband compression unit 280, although device 554 preferably uses a constant β
23 different from the constant α . The behavior of averaging device 554 is of course also
24 described by Equation (5) when β is substituted for α . The constant β is preferably
25 selected for device 554 so that the time constant of RMS level detector 544 closely
26 approximates the corresponding time constant specified by the BTSC standard for RMS
27 level detector 144 (shown in Figure 1). Averaging device 554 computes a time
28 weighted average of the signal on line 552a and applies the average to square root

1 device 556 via line 554a. Square root device 556 calculates the square root of the signal
2 on line 554a and thereby generates a signal on line 544a as a function of the RMS value
3 of the output signal generated by spectral bandpass filter 542.

4 The signal on line 544a is applied to the control terminal of variable emphasis
5 unit 536. Variable emphasis unit 536 performs processing that is partially analogous
6 to filter 136 (shown in Figure 1) of idealized encoder 100. As defined by the BTSC
7 standard, filter 136 has amplitude and phase responses that vary as a function of the
8 output signal generated by RMS level detector 144. One preferred way to implement
9 unit 536 so that it has similar variable responses is to use a digital filter having variable
10 coefficients that determine its transfer function and to select the value of the coefficients
11 during any given sample period, or group of sample periods, based on the value of the
12 signal on line 544a.

13 Figure 6 shows one embodiment of variable emphasis unit 536 which includes
14 a logarithmic generator 558, a variable emphasis filter 560, and a look up table LUT
15 562. The output signal generated by RMS level detector 544 is applied via line 544a
16 to logarithmic generator 558. The latter generates a signal on line 558a that is
17 representative of the logarithm of the signal on line 544a and applies this signal to LUT
18 562. LUT 562 generates an output signal selected from the LUT and representative of
19 filter coefficients to be used by variable emphasis filter 560. The coefficients thus
20 generated by LUT 562 are applied via line 562a to a coefficient selection terminal of
21 variable emphasis filter 560. The output signal generated by wideband compression unit
22 280 is applied to an input terminal of variable emphasis filter 560 via line 281. Variable
23 emphasis filter 560 generates the output signal of spectral compression unit 290 which
24 is applied to the input of fixed preemphasis filter 232b.

25 Variable emphasis filter 560 is designed to have a variable amplitude response
26 that closely matches the variable amplitude response of filter 136 (shown in Figure 1)
27 of idealized encoder 100. Variable emphasis filter 560 provides a similar variable
28 response by using a variable coefficient transfer function (i.e., the coefficients of the

1 transfer function $H(z)$ of filter 560 are variable) and by allowing LUT 562 to select the
2 value of the coefficients during intervals based on the sample period. As will be
3 described in greater detail below, LUT 562 stores the values of the filter coefficients
4 used by filter 560, and during each sample period, or during any selected group of
5 sample periods, LUT 562 selects a set of filter coefficients as a function of the output
6 signal generated by logarithmic generator 558 on line 558a. In one preferred
7 embodiment, variable emphasis filter 560 is implemented as a first order IIR filter
8 having a transfer function $H(z)$ that is described by the formula shown in the following
9 Equation (6).

10
$$H(z) = \frac{b_0 + b_1 z^{-1}}{1 + a_1 z^{-1}} \quad (6)$$

11 in which the filter coefficients b_0 , b_1 , and a_1 are variables that are selected by LUT 562.
12 Methods of selecting the values for the filter coefficients used by filter 560 as well as
13 by the other filters of encoder 200 will be discussed below.

14 In Figure 6, logarithmic generator 558 and square root device 556 are shown,
15 for convenience, as two separate components. However, those skilled in the art will
16 appreciate that these two components may be implemented using a single device, such
17 as a LUT, or alternatively using processing components that calculate a Tayler series
18 polynomial approximation of the logarithm of the signal on line 554a and by then
19 dividing this value by two. Similarly, in alternative implementations, the functions
20 performed by logarithmic generator 558, square root device 556, and LUT 562 may be
21 incorporated into a single device.

22 As stated above, high pass filters 212, 214 (shown in Figure 3) are useful in
23 blocking DC components so as to prevent encoder 200 from exhibiting a behavior
24 known as "ticking". In the context of a stereophonic encoder, ticking refers to
25 relatively low frequency oscillatory behavior of the encoder caused when there is no
26 signal present at the left and right channel audio inputs. The desired behavior of a
27 stereophonic system when there is no signal present at the audio inputs is to remain

1 silent; however, an encoder connected through a decoder to loudspeakers and exhibiting
2 ticking causes the loudspeakers to emit an audible sound, referred to as a "tick", with
3 a somewhat regular period that is partially dependent on the time constant of the RMS
4 level detector in the wideband compressor. More particularly, in encoder 200, when
5 only very low level signals are present at the audio inputs, and when there is a D.C.
6 component, or an offset, present in the signal on line 239, wideband compression unit
7 280 tends to behave in an unstable fashion that causes ticking.

8 Consider the case where only a low level audio signal is present on line 239.
9 In such a case, the output of RMS level detector 450 on line 450a becomes very small,
10 which in turn causes the gain of multiplier 434 to become very large. If such a low
11 level audio signal on line 239 is constant in its amplitude, the wideband compression
12 unit 280 reaches a steady-state condition after some time (determined by the time
13 constant α applied to multiplier 460), because the encoded difference signal is fed back
14 on line 240 to the wideband compression unit 280. Because the feedback is arranged
15 to be negative, when the audio signal on line 239 increases in its amplitude, the signal
16 on line 450a increases, which in turn causes the gain of multiplier 434 to decrease.
17 When the audio signal on line 239 decreases in its amplitude, the signal on line 450a
18 decreases, which in turn causes the gain of multiplier 434 to increase.

19 However, should there be a significant dc signal present on line 239 in addition
20 to a low level audio signal, the dc signal is blocked from the feedback process by the
21 action of wideband bandpass filter 448, which has zero response to dc signals. In
22 particular, any dc present in the encoded difference signal at line 240 is blocked by filter
23 448, and is not sensed by RMS level detector 450. Any dc signal present on line 239
24 will be amplified by multiplier 434 along with any audio signal present on line 239, but
25 the amplification factor or gain will be determined only by the audio signal amplitude
26 as sensed by RMS level detector 450 after filtering by filter 448.

27 As noted above, whenever the amplitude of the audio signal on line 239 varies,
28 the gain of multiplier 434 varies inversely. During such variations in gain, any dc

1 present on line 239 will also be subjected to variable amplification, in effect modulating
2 the dc signal, thereby producing an ac signal. In this fashion such dc signals may be
3 modulated so as to create significant audio-band signals which will not be rejected by
4 filter 448, and are therefore sensed by detector 450. When the audio signal on line 239
5 is small compared to the dc on line 239, small variations in the audio signal level, which
6 cause changes in the gain of amplifier 434, can cause a large change in the dc level
7 (which amount to an ac signal) at line 281 through this modulation process. The ac
8 signal produced tends to increase the overall signal which passes through filter 448,
9 regardless of whether the audio signal variation that gave rise to the ac signal was an
10 increase or decrease in signal level. In particular, should the level of the audio signal
11 on line 239 decrease, the negative feedback process normally increases the gain of
12 multiplier 434. However, if a sufficient dc signal is present in line 239, a decrease in
13 audio signal on line 239 can cause an increase in the signal sensed by detector 450,
14 forcing the gain of multiplier 434 to decrease. In this fashion, the negative feedback
15 process is reversed, and the feedback becomes positive.

16 Such positive feedback will only persist so long as the modulated dc signal at line
17 281 is sufficiently large compared to any audio signal present on line 281, when
18 weighted by the response of all the filters and signal modifiers between line 281 and the
19 output of filter 448. Once the gain of multiplier 434 decreases sufficiently such that the
20 modulated dc signal in line 281 no longer provides a significant input to detector 450,
21 the feedback reverts to its normal negative sense. In accordance with the time constant
22 of detector 450, the system will re-acquire an appropriate gain level based on the level
23 of the audio signal in line 239. But, if sufficient dc remains in the signal in line 239,
24 the cycle will repeat itself once the gain of multiplier 434 increases sufficiently. During
25 each such period of positive feedback, a sharp change in the dc level of line 281 is
26 produced. This change is audible, and sounds somewhat similar to the 'tick' of a clock.
27 Since such dc changes will occur with some regularity, based on the time constant of
28 detector 450, the phenomenon is often referred to as 'ticking'.

1 One method of preventing ticking is to remove any dc components present in the
2 input signal to encoder 200. This is accomplished by high pass filters 212 and 214.
3 Further, high pass filters 212 and 214 help to maximize the dynamic range of encoder
4 200 by removing dc components which otherwise may use up valuable dynamic range.

5 As stated above and as shown in Figure 3, low pass filter 238 is preferably
6 implemented as two filters 238a and 238b. Splitting filter 238 in this fashion provides
7 several advantages. If filter 238a were eliminated, and the entire filter 238 were located
8 after clipper 254 (i.e., in the location of filter 238b) then any components above 15 kHz
9 on the audio input signals may cause instability in the wideband compression unit 280
10 similar to the above-described ticking behavior. This occurs because any signal
11 components above 15 kHz on line 239 will be amplified by multiplier 434 (shown in
12 Figure 5) and because such components will not be sensed by RMS level detector 450
13 since such components are filtered out by the low pass filter following clipper 254
14 (shown in Figure 3). Since detector 450 increases the gain of multiplier 434 when it
15 senses the absence of a signal, the gain of multiplier 434 can become relatively large
16 when the signal on line 239 consists of little audio signal (under 15kHz) information,
17 but significant high-frequency (over 15kHz) information. Multiplier 434 then amplifies
18 the high-frequency information, which can generate large signals that are likely to be
19 clipped by components in processing section 230. This clipping can produce harmonics
20 which may alias to low frequencies that will be sensed by RMS level detector 450
21 causing the system to tick as described previously. Alternatively, if filter 238b were
22 eliminated and the entire filter 238 were located before fixed preemphasis filter 232a
23 (i.e., in the location of filter 238a) then high frequency artifacts generated by clipper
24 254 would be included in the encoded difference signal and could interfere with the pilot
25 tone in the composite signal. Therefore, splitting filter 238 as shown provides an
26 optimal arrangement whereby filter 238a prevents ticking in compression unit 280 and
27 filter 238b filters high frequency artifacts that may be generated by clipper 254.
28

Fixed preemphasis filter 232 is also preferably split into two filters 232a, 232b as shown in Figure 3. Filter 232 typically requires relatively large gain at high frequencies, as is specified in the BTSC standard, and using only a single section to implement filter 232 increases the likelihood of filter 232 causing clipping. It is advantageous to apply some of the gain of filter 232 on the input side of wideband compression unit 280 (with filter 232a) and to apply some of the gain of filter 232 on the output side of wideband compression unit 280 (with filter 232b). Since unit 280 normally compresses its input signal, distributing the gain of filter 232 around the compression provided by unit 280 decreases that the likelihood that the gain of filter 232 will cause an overflow condition.

To minimize size, power consumption, and cost, encoder 200 is preferably implemented using a single digital signal processing chip. Encoder 200 has been successfully implemented using one of the well known Motorola DSP 56002 digital signal processing chips (this implementation shall be referred to hereinafter as the "DSP Embodiment"). The Motorola DSP 56002 is a fixed point twenty-four bit chip, however, other types of processing chips, such as floating point chips, or fixed point chips having other word lengths, could of course be used. The DSP Embodiment of encoder 200, uses a sampling frequency f_s that is equal to three times the pilot frequency f_H (i.e., $f_s = 47202$ Hz). The following Table 1 lists all of the filter coefficients used in the DSP Embodiment of encoder 200 except those used in variable emphasis filter 560.

TABLE 1

Low Pass Filter (Section #1) 310 (Equation 4)	Low Pass Filter (Section #2) 312 (Equation 4)
$b_0=0.18783270$	$b_0=0.44892888$
$b_1=0.36310206$	$b_1=0.70268024$
$b_2=0.18783270$	$b_2=0.44892888$
$a_1=-0.388832539$	$a_1=0.12638618$

1	$a_2=0.12709286$	$a_2=0.47415181$
2	Low Pass Filter (Section #3) 314	Low Pass Filter (Section #4) 316
3	(Equation 4)	(Equation 4)
4	$b_0=0.70674027$	$b_0=0.85733126$
5	$b_1=0.87637648$	$b_1=0.91505047$
6	$b_2=0.70674027$	$b_2=0.85733126$
7	$a_1=0.53702472$	$a_1=0.74320197$
8	$a_2=0.75298490$	$a_2=0.89832289$
9	Low Pass Filter (Section #5) 318	Wideband Bandpass Filter 448
10	(Equation 4)	(Equation 4)
11	$b_0=0.92737972$	$b_0=-0.02854672$
12	$b_1=0.92729649$	$b_1=-0.18789051$
13	$b_2=0.92737972$	$b_2=0.21643723$
14	$a_1=0.82951974$	$a_1=-1.75073141$
15	$a_2=0.97259237$	$a_2=0.75188028$
16	Fixed Preemphasis Filter 238a	Fixed Preemphasis Filter 238b
17	(Equation 2)	(Equation 2)
18	$b_0=9.50682180$	$b_0=4.357528$
19	$b_1=-9.00385663$	$b_1=-3.24843271$
20	$a_1=-0.497064357$	$a_1=0.10881833$
21	Spectral Bandpass Filter	Spectral Bandpass Filter
22	(Section #1) 542a	(Section #2) 542b
23	(Equation 4)	(Equation 4)
24	$b_0=0.646517841$	$b_0=0.850281278$
25	$b_1=0.649137616$	$b_1=-0.850247036$
26	$b_2=0.0$	$b_2=0.0$

1	$a_1=0.557821757$	$a_1=-0.602159890$
2	$a_2=0.0$	$a_2=0.0$
3	Spectral Bandpass Filter	Static Phase Equalization Filter 224
4	(Section #3) 542c	(Equation 3)
5	(Equation 4)	
6	$b_0=0.597678418$	$a_0=0.9029$
7	$b_1=-1.195357770$	
8	$b_2=0.597679348$	
9	$a_1=-0.776566094$	
10	$a_2=0.352824276$	
11	75 μ s preemphasis filter 222	High Pass Filters 212, 214
12	(Equation 2)	(Equation 1)
13	$b_0=4.57030583$	$a_1=-0.999$
14	$b_1=-3.43823487$	
15	$a_1=0.131778883$	
16		

In the DSP Embodiment of encoder 200 the value of the constant α that is used by averager 454 (shown in Figure 5) in wideband compression unit 280 is set equal to 0.0006093973517, and the value of the constant β that is used by averager 554 (shown in Figure 6) in spectral compression unit 290 is set equal to 0.001825967. Further, the values of Gain C and Gain D used by amplifiers 540 and 446, respectively, in the spectral and wideband compression units are set equal to 0.5011872 and 0.08984625, respectively, to insure that the DSP Embodiment of encoder 200 performs similarly to encoder 100.

Figure 7 shows a flow chart 700 that describes one preferred method for pre-calculating all the sets of filter coefficients used by variable emphasis filter 560 (shown in Figure 6) in the DSP Embodiment of encoder 200. Prior to operation of encoder 200, all the sets of filter coefficients used by filter 560 are pre-calculated (e.g., by a general purpose digital computer) and are loaded into LUT 562. In the DSP

Embodiment of encoder 200, filter 560 has a transfer function $H(z)$ that is described by Equation (6) so flow chart 700 describes the calculation of the coefficients b_0 , b_1 , and a_1 . As specified in the BTSC standard, the transfer function of $S(f,b)$ of analog filter 136 (shown in Figure 1) to which filter 560 partially corresponds, is described by the formula shown in the following Equation (7).

$$S(f, b) = \frac{1 + \frac{\left(\frac{jf}{F}\right)(b+51)}{(b+1)}}{1 + \frac{\left(\frac{jf}{F}\right)(1+51b)}{(b+1)}} \quad (7)$$

in which F is equal to 20.1 kHz.

The first step in flow chart 700 in an initialization step 710 during which several variables are initialized. Specifically, the sampling frequency f_s is set equal to 47202 Hz, and the period T is set equal to $1/f_s$. The variable W is a digital version of the variable F used in Equation (7) and is set equal to $\pi(20.1 \text{ kHz})/f_s$. The variable dBRANGE represents the desired signal range of the RMS detectors in the spectral compression unit, and for the DSP Embodiment dBRANGE is set equal to 72.25 dB. The variable dBRES relates to the sensitivity of filter 560 to changes in the energy level of the encoded difference signal. In the DSP Embodiment of encoder 200, dBRES is set equal to 0.094 dB so that filter 560 will use coefficients based on the value of the signal on line 558a quantized to the nearest 0.094 dB. The variable N equals the total number of sets of filter coefficients used in filter 560 and N is calculated by dividing the sensitivity (dBRES) into the range (dBRANGE) and rounding to the nearest integer. In the DSP Embodiment, N is equal to 768 although those skilled in the art will appreciate that this number can be changed which will vary the sensitivity or the range. In the DSP Embodiment, LUT 562 stores 769 sets of coefficients for filter 560, and of course if N is increased, a larger LUT will be used to store the extra sets of filter

1 coefficients. Further, those skilled in the art will appreciate that logarithmic generator
2 558 scales the signal on line 558a and thereby reduces the number of filter coefficient
3 sets stored by LUT 562, for a given minimum quantization of the value of the signal on
4 line 558a. However, in other embodiments, logarithmic generator 558 may be
5 eliminated and LUT 562 may store a correspondingly larger number of filter coefficient
6 sets. Finally, the variables Scale and Address are set equal to 32 and zero, respectively.
7 The variable Scale, which is only used in fixed point implementations, is selected so that
8 all the filter coefficients have a value greater than or equal to negative one and less than
9 one (where the filter coefficients are represented in twos complement).

10 Following initialization step 710, a coefficient generation step 720 is executed.
11 During the first execution of step 720, variables $b_0(0)$, $b_1(0)$, and $a_1(0)$ are calculated
12 which correspond to values of the coefficients b_0 , b_1 , and a_1 that are to be stored at
13 address location zero of LUT 562. Following this execution of step 720, an
14 incrementing step 730 is executed during which the value of the variable Address is
15 incremented. Following step 730 a comparison step is executed during which the values
16 of the variables Address and N are compared. If Address is less than or equal to N,
17 then steps 720, 730, and 740 are reexecuted iteratively so that values of the coefficients
18 b_0 , b_1 , and a_1 are calculated for each of the 769 addresses of LUT 562. When step 740
19 detects that the value of Address is greater than N, then all 769 sets of coefficients have
20 been calculated and execution of flow chart 700 proceeds to a concluding step 750.

21 In coefficient generation step 720, the variable dBFS corresponds to the output
22 of logarithmic generator 558. As the value of the variable Address ranges from zero
23 to 769, the value of dBFS ranges from about -72.25 to zero dB corresponding to the
24 signal range of about 72.25 dB provided by the DSP Embodiment of encoder 200
25 (where zero dB corresponds to the full modulation). The variable RMSd corresponds
26 to the output of the analog RMS level detector 144 (shown in Figure 1), and as the
27 variable Address ranges from zero to 769, the value of RMSd ranges from about -36 to
28 36 dB corresponding to the signal range of 72 dB provided by typical prior art analog

BTSC encoders. The variable RMSb is a linear version of the variable RMSd, and RMSb corresponds to the variable b in the transfer function $S(f,b)$ described in Equation (7). The variables K1 and K2 correspond to the $(b+51)/(b+1)$ and the $(51b+1)/(b+1)$ terms, respectively, in Equation (7). The coefficients b_0 , b_1 , and a_1 are calculated as shown in step 720 using the variables K1, K2, W, and Scale.

Figure 8A shows a block diagram that illustrates one method of using the DSP Embodiment in an analog system, and in Figure 8A, all components that are implemented in the 56002 integrated circuit are indicated at 200a. The analog system supplies analog left and right channel audio input signals (shown in Figure 8A as "L" and "R", respectively) and these signals are applied to the inputs of sixteen bit analog-to-digital converters 810 and 812, respectively. Converters 810, 812 sample their analog input signals using a sampling frequency f_s that is equal to 47,202 Hz (i.e., $3f_H$) and converters 810, 812 thereby generate sequences of sixteen bit digital samples that are representative of the left and right channel audio input signals, respectively. The signals generated by converters 810 and 812 are applied to encoder 200a where they are received by modules 292 and 294, respectively. Modules 292, 294 are "divide by sixteen" modules (which divide the amplitude of their inputs by a factor of 16) and therefore generate output signals that are equal to their input signals divided by sixteen. Since division by any power of two is easily accomplished in a digital system by using a shift register, modules 292, 294 are implemented as shift registers that shift their inputs by four binary places.

As stated above, the 56002 chip is a fixed point twenty-four bit processor, and the samples applied to the chip by converters 810, 812 are in twos complement representation. Modules 292, 294 divide the samples generated by converters 810, 812 by sixteen and thereby place each of the samples in the middle of a twenty-four bit word. So in every sample generated by modules 292, 294, the four most significant bits are sign bits and the four least significant bits are zeros, and the sixteen bits in the middle of the word correspond to one sample generated by one of the converters 810,

1 812. Padding each twenty-four bit word with sign bits at the high end and with zeros
2 at the low end in this fashion preserves accuracy and allows intermediate signals
3 generated by encoder 200a to exceed sixteen bits without causing an error condition such
4 as an overflow.

5 In encoder 200a, each bit of the twenty-four bit word corresponds roughly to 6dB
6 of signal range, and therefore modules 292, 294 correspond to -24 dB (i.e., negative 6
7 times 4) attenuators. If the analog input signals applied to converters 810, 812 are
8 considered for reference purposes as zero dB signals, then the signals generated by
9 modules 292, 294 are attenuated by 24 dB.

10 Input section 210 receives the twenty-four bit words generated by modules 292,
11 294 and generates therefrom the sum signal that is applied to the sum channel processing
12 section 220. The output signal generated by sum channel processing section 220 is
13 applied to a "times 16 module" (which may be considered as a 24 dB amplifier) 296.
14 Module 296 thereby compensates for the -24dB attenuators 292, 294 and brings the
15 output of sum channel processing section 220 back to 100% modulation (i.e., back to
16 "full scale"). The output signal generated by module 296 is applied to a sixteen bit
17 digital-to-analog converter 814 which in turn generates an analog conditioned sum
18 signal.

19 Input section 210 also generates the difference signal that is applied to the
20 difference channel processing section 230. As stated above, as a result of modules 292,
21 294, the difference signal may be considered as being attenuated by 24 dB. In the DSP
22 embodiment of encoder 200a, clipper 254 (shown in Figure 3) of the difference
23 processing section 230 includes an 18 dB amplifier (which is implemented as a multiply
24 by eight). That is, clipper 254 amplifies the signal generated by fixed preemphasis filter
25 232b by 18 dB and then clips this amplified signal so that the output signal generated
26 by clipper 254 will not exceed a number that is 6dB down from full modulation. The
27 signal applied from clipper 254 to low pass filter 238b therefore has one bit (or 6 dB)
28 of "headroom", so filter 238b may generate an output signal that is 6 dB greater than

1 its input signal without causing saturation. It is desirable to leave this one bit of
2 headroom because the transient response of filter 238b includes some ringing that may
3 cause it to temporarily generate an instantaneous output signal that is greater than its
4 instantaneous input signal and the headroom thereby prevents any ringing in filter 238b
5 from causing a saturation condition. Referring again to Figure 8A, the output signal
6 generated by filter 238b is applied to a sixteen bit digital-to-analog converter 816 which
7 in turn generates an output signal that is applied to a 6 dB analog amplifier 820. Both
8 D/A converters 814 and 816 are intended to be complete converters, which include the
9 well-known analog anti-image filters as part of their functionality. Anti-image filters
10 are analog filters applied to the analog signal following digital to analog conversion
11 which serve to attenuate any images of the desired signal which are mirrored about the
12 sample frequency and multiples thereof. Converters 814 and 816 are assumed to be
13 substantially identical to one another, running at the same sample rate and containing
14 substantially the same anti-image filtering. Such converters are commonly available in
15 commercial embodiments, such as the Crystal Semiconductor CS4328. Amplifier 820
16 amplifies its input signal by 6 dB and thereby brings the encoded difference signal back
17 up to full scale. While Figure 8A shows encoder 200a coupled to analog-to-digital
18 converters 810, 812 for receiving analog audio signals, in digital systems converters
19 810, 812 may of course be eliminated so that encoder 200a receives the digital audio
20 signals directly.

21 Figure 8B shows a block diagram of one preferred embodiment of a BTSC
22 encoder 200b constructed according to the invention and configured as part of an analog
23 system. Encoder 200b is similar to encoder 200a, however, in encoder 200b module
24 296 amplifies its input signal by 18 dB (by multiplying by 8) rather than by 24 dB as
25 in encoder 200a. The output signal generated by module 296 is a scaled version of the
26 conditioned sum signal and is shown in Figure 8B as S. Also, encoder 200b includes
27 a module 298 for amplifying the output signal generated by difference channel
28 processing section 230 by 6 dB (by multiplying by two). The output signal generated

1 by module 298 is a scaled version of the encoded difference signal and is shown in
2 Figure 8B as D. Further, encoder 200b includes a composite modulator 822 for
3 receiving the signals S and D and for generating therefrom a digital version of the
4 composite signal. The digital composite signal generated by modulator 822 is applied
5 to a digital-to-analog converter 818 the output of which is an analog version of the
6 composite signal. D/A converter 818 is intended to be a complete converter which
7 includes the aforementioned analog anti-image filter as part of its functionality. Such
8 converters are commonly available in commercial embodiments, such as the Burr-Brown
9 PCM1710. In the preferred embodiments, modules 292, 294, input section 210, sum
10 channel processing section 220, difference channel processing section 230, modules 296,
11 298, and composite modulator 822 are all implemented on a single digital signal
12 processing chip.

13 Since the composite signal is generated as a digital signal in encoder 200b,
14 module 298 is included to bring the output signal generated by difference channel
15 processing section 230 up to full scale rather than waiting until after digital-to-analog
16 conversion and using an analog amplifier such as amplifier 820 as is shown in Figure
17 8A. Also, since in the composite signal the conditioned sum signal is used at 50%
18 modulation, module 296 only amplifies its input signal by 18 dB so that the output
19 signal generated by module 296 is at half the amplitude of the output signal generated
20 by module 298.

21 Figure 9 shows a block diagram of one embodiment of composite modulator 822.
22 The latter receives the signals S and D and generates therefrom a digital version of the
23 composite signal. Modulator 822 includes two interpolators 910, 912, two digital low
24 pass filters 914, 916, a digital signal multiplier 918, and two digital signal adders 920,
25 922. The S and D signals are applied to respective inputs of the interpolators 910 and
26 912. Interpolators 910, 912, which are alternatively referred to as "up-samplers",
27 interpolate a new sample between every two consecutive samples applied to their inputs,
28 and thereby generate output signals having twice the sampling frequency as the input

1 signals S and D. The output signals generated by interpolators 910 and 912 are applied
2 to respective inputs of low pass filters 914 and 916. The latter remove images
3 introduced into the S and D signals by interpolators 910, 912. The filtered output signal
4 generated by filter 916 is applied to one input of signal multiplier 918 and a digital
5 oscillating signal as a function of $\cos[4\pi(f_H/f_s)n]$ is applied to the other input of
6 multiplier 918. Multiplier 918 thereby generates the amplitude modulated, double-
7 sideband, suppressed carrier version of the difference signal that is used in the
8 composite signal. The output signal generated by multiplier 918 is applied to one input
9 of signal adder 920 and the filtered output signal generated by filter 914 is applied to
10 the other input of signal adder 920. The latter generates an output signal by summing
11 the two signals present at its inputs and applies this signal to signal adder 922. A pilot
12 tone signal that oscillates as a function of $A\cos[2\pi(f_H/f_s)n]$ (where 'A' is a constant
13 representative of 10% of full scale modulation) is applied to the other input of signal
14 adder 922 which generates the digital composite signal by summing the two signals
15 present at its inputs.

16 Composite modulator 822 includes interpolators 910, 912 because the highest
17 frequency component in the composite signal is slightly less than $3f_H$ (as is shown in
18 Figure 2), and therefore the signals applied to the inputs of signal multiplier 918 and
19 signal adder 920 should have sample rates at least as large as $6f_H$ to satisfy the Nyquist
20 criteria. Because the sample rate at the output of composite modulator 822 is typically
21 higher than the sample rate of either the S or D signals, D/A converter 818 must be
22 capable of operating at such higher sample rates. If the input signals S and D applied
23 to composite modulator 822 have sample rates of $3f_H$ some form of interpolation (such
24 as that provided by interpolators 910, 912) should be provided to double the sample
25 rate. Of course, if sufficiently high sample rates are used throughout encoder 200b then
26 interpolators 910, 912 and low pass filters 914, 916 may be eliminated from modulator
27 822.

Figure 8C shows a block diagram of yet another embodiment of a BTSC encoder 200c constructed according to the invention. Encoder 200c is similar to encoder 200b (shown in Figure 8B) however, in encoder 200c module 298 is eliminated so that the signal generated by the difference channel processing section 230 is the signal D and is applied directly to composite modulator 822. Further, in encoder 200c, module 296 amplifies its input signal by 12 dB (by multiplying by 4) rather than by 18 dB as is done in encoder 200b. So in encoder 200c, the signals S and D are 6 dB down from the levels of those signals in encoder 200b. Composite modulator 822 therefore generates from these signals a version of the composite signal that is attenuated by 6 dB. This attenuated version of the composite signal is converted to an analog signal by digital-to-analog converter 818 and is then brought up to full scale by 6 dB analog amplifier 820. As with encoder 200b, encoder 200c is preferably implemented using a single digital signal processing chip.

The differences between encoders 200b and 200c represent design tradeoffs. As those skilled in the art will appreciate, when converting a digital signal to an analog signal with a digital-to-analog converter, insuring that the digital signal is at full scale tends to minimize any loss of signal-to-noise ratio that might occur as a result of the conversion. Encoder 200b minimizes the loss of signal-to-noise ratio as a result of the operation of converter 818 by using modules 296, 298 to insure that the digital version of the composite signal (generated by modulator 822) that is applied to converter 818 is at full scale. However, although converter 200b minimizes any loss of signal-to-noise ratio that might occur as a result of converter 818, encoder 200b also increases the likelihood that clipping might occur in the composite signal. Since the difference channel processing section 230 uses the relatively large gain provided by fixed preemphasis filter 232 (shown in Figure 3), it is possible for some clipping to occur in the path of the encoded difference signal. Encoder 200b uses module 298 to bring the D signal up to full scale and this essentially eliminates any headroom from the signal path of the D signal and thereby increases the chance that some clipping will occur. So

1 encoder 200b minimizes the loss of any signal-to-noise ratio that occurs as a result of
2 converter 818 at the cost of increasing the likelihood of clipping in the path of the
3 encoded difference signal. In contrast, encoder 200c preserves headroom in the path
4 of the encoded difference signal and thereby reduces the likelihood of clipping at the
5 cost of increasing the loss of signal-to-noise ratio that occurs as a result of operation of
6 converter 818.

7 Figure 8D shows a block diagram of yet another embodiment of a BTSC encoder
8 200d constructed according to the invention. Encoder 200d is similar to encoder 200a
9 (shown in Figure 8A) however, encoder 200d additionally includes a portion 822a of a
10 composite modulator. Portion 822a includes two interpolators 910, 912, two low pass
11 filters 914, 916, digital signal multiplier 918 and a digital signal adder 930. The S
12 signal generated by module 296 is applied to interpolator 910 which "up-samples" the
13 S signal and applies the up-sampled signal to low pass filter 914. The latter filters this
14 signal and applies the filtered signal to one input terminal of adder 930. A digital pilot
15 tone having twice the normal amplitude (i.e., $2A\cos 2\pi(f_H/f_S)n$) is applied to the other
16 input terminal of adder 930 which generates an output signal by summing the two
17 signals present at its input terminals. The D signal generated by difference channel
18 processing section 230 is applied to interpolator 912 which generates an up-sampled
19 signal that is applied to low pass filter 916. The latter filters this signal and applies the
20 filtered signal to one terminal of multiplier 918. A signal oscillating according to
21 $\cos 4\pi(f_H/f_S)n$ is applied to the other terminal of multiplier 918 which generates an output
22 signal by multiplying the two signals present at its input terminals. As with encoders
23 200a-c, encoder 200d is preferably implemented using a single digital signal processing
24 chip.

25 Encoder 200d is preferably used in conjunction with two digital-to-analog
26 converters 932, 934, an analog -6 dB attenuator 936, an analog 6 dB amplifier 938, and
27 an analog adder 940. The output signal generated by adder 930 is applied to converter
28 932 which generates an analog signal that is applied to attenuator 936. The output

1 signal generated by multiplier 918 is applied to converter 934 which generates an analog
2 signal that is applied to amplifier 938. The signals generated by attenuator 936 and
3 amplifier 938 are applied to input terminals of signal adder 940 which sums these
4 signals to generate the analog composite signal. D/A converters 932 and 934 are
5 intended to be complete converters which include the aforementioned analog anti-image
6 filters as part of their functionality. Converters 932 and 934 are assumed to be
7 substantially identical to one another, running at the same sample rate and containing
8 substantially the same anti-image filtering. Such converters are commonly available in
9 commercial embodiments, such as the Burr Brown PCM1710.

10 It is also possible to eliminate interpolator 910 and low pass filter 914 from
11 Figure 8D, and run D/A converter 932 at a sample rate equal to that of the sum channel
12 processing section 220. However, to do so is generally not practical because
13 inexpensive, commonly available D/A converters are usually available in pairs housed
14 within a single integrated circuit. Such paired D/A converters naturally operate at the
15 same sample rate. While it is possible to reduce DSP complexity by eliminating
16 interpolator 910 and low pass filter 914 from Figure 8D, doing so would also likely
17 increase the cost and complexity of the overall design because a simple stereo D/A
18 converter could no longer be used for both D/A converters 932 and 934.

19 Encoder 200d represents one combination of the features of encoders 200b and
20 200c. Encoder 200d uses module 296 to bring the S signal up to full scale so as to
21 minimize any loss of signal-to-noise ratio that might occur as a result of the operation
22 of converter 932. Encoder 200d also preserves 6 dB of headroom in the signal path of
23 the D signal and therefore reduces the likelihood of any loss of accuracy due to clipping.
24 Although encoder 200d includes more components than either of encoders 200b and
25 200c, encoder 200d both minimizes loss of signal-to-noise ratio and the likelihood of
26 clipping.

27 Figure 10 shows a block diagram of a preferred embodiment of sum channel
28 processing section 220a and difference channel processing section 230a for use in

1 encoder 200 (and these sections 220a, 230a may of course be used in encoders 200a-d).
2 Processing sections 220a, 230a are similar to the above-described sections 220, 230,
3 however, section 220a additionally includes dynamic phase equalization filter 1010, and
4 section 230a additionally includes a dynamic phase equalization filter 1012. In the
5 illustrated embodiment, the output signals generated by static phase equalization filter
6 228 and fixed preemphasis filter 232a are applied to the input terminals of dynamic
7 phase equalization filters 1010 and 1012, respectively, and the output signal generated
8 by logarithmic generator 558 on line 558a is applied to the control terminals of filters
9 1010, 1012. The output signals generated by filters 1010 and 1012 are applied to low
10 pass filter 224 and to wideband compression unit 280, respectively.

11 Dynamic phase equalization filters 1010, 1012 are used to compensate for phase
12 errors introduced by variable emphasis filter 560 which is used in spectral compression
13 unit 290. The phase response of variable emphasis filter 560 is preferably matched as
14 closely as is possible to that of variable emphasis filter 136 (shown in Figure 1).
15 However, due to the variable, signal dependent, nature of variable emphasis filter 136,
16 it is extremely difficult to design variable emphasis filter 560 so that its phase response
17 is matched to that of variable emphasis filter 136 for all pre-emphasis/de-emphasis
18 characteristics, which in turn varies with signal level. Therefore in typical embodiments
19 of encoder 200, the phase responses of variable emphasis filter 560 and variable
20 emphasis filter 136 diverge as a function of the signal level. Dynamic phase
21 equalization filters 1010, 1012 preferably introduce compensatory phase errors into the
22 sum and difference channel processing sections to compensate for the divergence
23 between variable emphasis filter 560 and variable emphasis filter 136.

24 Dynamic phase equalization filters 1010, 1012 therefore perform a function that
25 is similar to that performed by static phase equalization filter 228. However, whereas
26 filter 228 compensates for phase errors that are independent of the level of the encoded
27 difference signal, filters 1010, 1012 compensate for phase errors that are dependent on
28 this signal level. Filters 1010, 1012 are preferably implemented as "all pass" filters

1 having relatively flat magnitude responses and selected phase responses. Dynamic phase
2 equalization filters are included in both the sum and difference processing sections
3 because a phase delay may be required in either the sum or difference channel to
4 compensate for the phase error introduced by variable emphasis filter 560. In preferred
5 embodiments, filters 1010, 1012 are implemented in a similar fashion as variable
6 emphasis unit 536 and include a filter having a variable coefficient transfer function and
7 a LUT for selecting the values of the filter coefficients during any particular interval.
8 The signal generated by logarithmic generator 558 on line 558a is preferably applied to
9 the control terminals of filters 1010, 1012 and selects the filter coefficients used by
10 those filters.

11 Digital encoder 200 has been discussed in connection with certain particular
12 embodiments, however, those skilled in the art will appreciate that variations of these
13 embodiments are also embraced within the invention. For example, variable emphasis
14 unit 536 (shown in Figure 6) has been discussed in terms of being implemented using
15 a variable emphasis filter 560 and a LUT 562. However, rather than precomputing all
16 the possible coefficients for filter 560 and storing them in LUT 562, it may be
17 preferable for other implementations of variable emphasis unit 536 to eliminate LUT
18 562 and to instead include components for calculating the filter coefficients in real time.
19 Those skilled in the art will appreciate that such considerations represent a tradeoff
20 between memory resources (such as are used by a LUT for storing filter coefficients)
21 and computing resources (such as are used by components for calculating filter
22 coefficients in real time) and may be resolved differently in any particular
23 implementation of encoder 200. Similar considerations apply to square root devices 456
24 and 556, reciprocal generator 458, and logarithmic generator 558 (shown in Figures 5
25 and 6) which may alternatively use memory resources (e.g., a LUT for storing all the
26 values) or processing resources (e.g., for calculating a Taylor series polynomial
27 approximation). In yet other embodiments, any or all of the components in encoder

1 200 may be implemented using individual hardware components or alternatively as
2 software modules running on a general or specific purpose computer.

3 Another example of variations of encoder 200 that are embraced within the
4 invention relates to scaling modules 292, 294 (shown in Figure 8B). These modules are
5 particularly relevant to fixed point implementations of encoder 200. In floating point
6 implementations there is no need to pad each sample with zeros and sign bits to prevent
7 overflow and these modules can therefore be eliminated from floating point
8 implementations. As a further example, the static phase equalization filter 228 (shown
9 in Figure 10) has been discussed in terms of compensating for phase errors introduced
10 by filter 232a, however, filter 228 may be alternatively used to compensate for other
11 phase errors introduced by other components in the difference channel processing
12 section 230a. Still further, filters 228 and 1010 may be implemented as a single filter.

13 Therefore, since certain changes may be made in the above apparatus without
14 departing from the scope of the invention herein involved, it is intended that all matter
15 contained in the above description or shown in the accompanying drawing shall be
16 interpreted in an illustrative and not a limiting sense.